We claim:

1. A MOS transistor in a single-transistor memory cell, comprising:

a semiconductor substrate having a substrate surface, a first conductive region and a second conductive region;

a gate oxide disposed on said substrate surface;

a gate disposed on said gate oxide over an area between said first conductive region and said second conductive region; and

an insulating spacer disposed on said side wall of said gate, said spacer acting as an oxidation barrier;

said gate oxide insulating said gate from said semiconductor substrate and having a thickened area in a region below said side wall of said gate.

2. The MOS transistor according to claim 1, wherein said insulating spacer is a silicon nitride spacer.

3. The MOS transistor according to claim 2, wherein said gate includes a layer selected from the group consisting of a tungsten silicide layer and a polysilicon layer.

4. The MOS transistor according to claim 2, wherein said gate includes a tungsten silicide layer and a polysilicon layer.

5. The MOS transistor according to claim 1, wherein said gate includes a layer selected from the group consisting of a tungsten silicide layer and a polysilicon layer.

6. The MOS transistor according to claim 1, wherein said gate includes a tungsten silicide layer and a polysilicon layer.

7. A selection transistor in a DRAM memory cell, comprising the MOS transistor according to claim 6.

8. A selection transistor in a DRAM memory cell, comprising the MOS transistor according to claim 1.